What is claimed is:

1. The creation of a butt contact opening for high-density memory cells, comprising:

providing a substrate, the substrate having been provided over an active surface area there-of with:

(i) at least one patterned and etched layer of gate material forming a gate electrode adjacent to which a butt contact opening is to be created;

(ii) LDD impurity implants self-aligned with the at least one patterned and etched layer of gate material; and

(iii) a first and a second gate spacer over sidewalls of the at least one patterned and etched layer of gate material, the second gate spacer overlying a sidewall of the at least one patterned and etched layer of gate material adjacent to which the butt contact opening is to be created;

depositing an etch blocking mask comprising etch blocking material over the substrate, including the at least one patterned and etched layer of gate material, exposing the second gate spacer;

etching the second gate spacer in accordance with the etch blocking mask;

removing the etch blocking mask;

performing S/D implant into the active surface of the substrate over which a butt contact opening is to be created; and

complete processing of the substrate for the creation of the high-density memory cell.

2. The method of claim 1, the gate material preferably comprising polysilicon.

3. The method of claim 1, the gate spacers preferably comprising silicon nitride.

4. The method of claim 1, the LDD impurity implants being for NMOS devices and preferably comprising As or P, implanted with an energy of between about 2 to 60 KeV and a dose of between about 1E13 to 2E15 atoms/cm^2.

5. The method of claim 1, the LDD impurity implants being for PMOS devices and preferably comprising BF_2 or B, implanted with an energy of between about 1 to 60 KeV and a dose of between about 1E13 to 2E15 atoms/cm^2.

6. The method of claim 1, the S/D implant being a N-type S/D region comprising As or P, implanted with an energy between about 10 and 100 KeV and a dose between about 1E14 to 5E16 atoms/cm^2.

7. The method of claim 1, the S/D implant being a P-type S/D region comprising boron or BF2, implanted with an energy between about 5 and 200 KeV and a dose between about 1E14 to 5E16 atoms/cm^2.

8. The method of claim 1, the etch blocking mask material comprising photoresist.

9. The method of claim 1, the etch blocking mask comprising a pattern enlargement of a butt contact opening.

10. The method of claim 9, the enlargement comprising increasing a sizing rule for a butt contact opening by between about 0.005 and 0.2 μm.

11. The method of claim 1, the complete processing of substrate for the creation of the high-density memory cell comprising:

saliciding contact surfaces of the at least one patterned and etched layer of gate material and the etched second gate spacer;

depositing a layer of etch stop material over the substrate, including the at least one patterned and etched layer of gate material and the etched second gate spacer;

depositing a layer of dielectric over the etch stop layer; and

patterning and etching the layer of dielectric and the etch stop layer, creating a butt contact opening through the layer of dielectric and the layer of etch stop layer, creating a conventional contact opening through the layer of dielectric, the butt contact opening being adjacent to the etched second gate spacer.

12. The creation of a butt contact opening for high-density memory cells, comprising:

providing a substrate, the substrate having been provided with:

(i) at least one patterned and etched layer of gate material forming the body of a gate electrode adjacent to which a butt contact opening is to be created;

(ii) high-density, two masked high energy LDD impurity implants comprising N-type (NLDD) or P-type (PLDD) implants;

(iii) a first and a second gate spacer over sidewalls of the at least one patterned and etched layer of gate material, the second gate spacer overlying a sidewall of the at least one patterned and etched layer of gate material adjacent to which the butt contact opening is to be created; and

(iv) a high-density, high energy well implant over the surface of which the butt contact opening is to be created;

depositing an etch blocking mask of etch blocking material comprising an enlarged sizing rule over the substrate, including the at least one patterned and etched layer of gate material, at least exposing the second gate spacer;

etching the second gate spacer in accordance with the etch blocking mask;

removing the etch mask;

performing an S/D impurity implant into the substrate; and

completing processing of the substrate for creation of the high-density memory cell.

13. The method of claim 12, the gate material preferably comprising polysilicon.

14. The method of claim 12, the gate spacers preferably comprising silicon nitride.

15. The method of claim 12, the high-density LDD impurity implants being for NMOS devices and preferably comprising As or P, implanted with an energy of between about 2 to 60 KeV and a dose of between about 1E13 to 2E15 atoms/cm^2.

16. The method of claim 12, the high-density LDD impurity implants being for PMOS devices and preferably comprising BF_2 or B, implanted with an energy of between about 1 to 60 KeV and a dose of between about 1E13 to 2E15 atoms/cm^2.

17. The method of claim 12, the high-density well implant being a N-type implant comprising As or P, implanted with an energy between about 10 and 100 KeV and a dose between about 1E14 to 5E16 atoms/cm^2.

18. The method of claim 12, the high-density well implant being a P-type implant comprising boron or BF2, implanted with an energy between about 5 and 200 KeV and a dose between about 1E14 to 5E16 atoms/cm^2.

19. The method of claim 12, the etch blocking mask material comprising photoresist.

20. The method of claim 12, the enlarged sizing rule comprising a pattern of an enlarged butt contact opening.

21. The method of claim 12, the enlarged sizing rule comprising increasing a sizing rule for a butt contact opening by between about 0.005 and 0.2 μm.

22. The method of claim 12, the complete processing of substrate for the creation of the high-density memory cell comprising:

saliciding contact surfaces to the at least one patterned and etched layer of gate material, including the etched second gate spacer;

depositing a layer of etch stop material over the substrate, including the at least one patterned and etched layer of gate material and the etched second gate spacer;

depositing a layer of dielectric over the layer of etch stop material; and

patterning and etching the layer of dielectric and the etch stop layer, creating a butt contact opening through the layer of dielectric and the layer of etch stop layer, creating a conventional contact opening through the layer of dielectric, the butt contact opening being adjacent to the etched second gate spacer.

23. A butt contact opening for high-density memory cells, comprising:

a silicon semiconductor substrate:

at least one patterned and etched layer of gate material forming a gate electrode;

a first gate spacer over a first sidewall of the at least one patterned and etched layer of gate material, the first gate

spacer being opposite to a second sidewall of the at least one patterned and etched layer of gate material;

LDD and S/D impurity implants self-aligned with the at least one patterned and etched layer of gate material, the S/D impurity implant underlying the LDD impurity implant, the LDD implant and the S/D implant underlying and surrounding a corner where the second sidewall of the etched layer of gate material interfaces with the active surface of the substrate over which a butt contact is provided;

a well implant underlying the butt contact opening;

a layer of etch stop material over the substrate, including the at least one patterned and etched layer of gate material;

a layer of dielectric over the layer of etch stop material;

a butt contact opening through the layer of dielectric and the layer of etch stop material, a conventional contact opening through the layer of dielectric, the butt contact opening comprising and laterally extending from the second sidewall of the at least one patterned and etched layer of gate material; and

the butt contact opening and the conventional contact opening having been filled with a conductive interconnect.

24. The butt contact opening of claim 23, additionally comprising salicided contact surfaces.

25. The butt contact opening of claim 23, the gate material preferably comprising polysilicon.

26. The butt contact opening of claim 23, the gate spacers preferably comprising silicon nitride.

27. The butt contact opening of claim 23, the enlarged sizing rule comprising a pattern of an enlarged butt contact opening.

28. The butt contact opening of claim 23, the enlarged sizing rule comprising an increased a sizing rule, increased by between about 0.005 and 0.2 μm.

29. The creation of a semiconductor device having a butt contact opening for high-density memory cells, comprising:

providing a substrate, an active region having been defined for the substrate;

performing N/P well implants into the surface of the substrate;

providing a patterned layer of gate electrode material over the active surface of the substrate, the patterned layer of gate electrode material having a first and a second sidewall, a butt contact having to be created comprising and laterally extending from the second sidewall;

performing LDD implant into the substrate, self-aligned with the patterned layer of gate electrode material, the LDD implant penetrating under and surrounding a corner where the second sidewall of the patterned layer of gate electrode material intersects with the active surface of the substrate over which a butt contact is to be created;

forming gate spacers over the first and the second sidewall of the patterned layer of gate electrode material;

creating an etch blocking mask over the patterned layer of gate electrode material, an opening through the etch blocking mask comprising and laterally extending from the second sidewall of the patterned layer of gate electrode material thereby exposing the spacer created over the second sidewall of the patterned layer of gate electrode material;

etching the spacer formed over the second sidewall of the patterned layer of gate electrode material in accordance with the etch blocking mask;

removing the etch blocking mask;

performing S/D implant into the substrate, the S/D implant underlying the LDD implant thereby providing that the S/D implant additionally penetrates under and surrounds the corner where the second sidewall of the patterned layer of gate electrode material intersects with the active surface of the substrate over which a butt contact is to be created;

performing salicidation of contact surfaces of the semiconductor device;

depositing an etch stop layer over salicided contact surface of the semiconductor device;

depositing a layer of dielectric over the etch stop layer;

patterning the deposited layer of dielectric to form therethrough a butt contact and a standard contact opening; and

filing the butt contact and a standard contact opening with a conductive material.

30. The method of claim 29, the gate electrode material preferably comprising polysilicon.

31. The method of claim 29, the gate spacers preferably comprising silicon nitride.

32. The method of claim 29, the LDD impurity implant being for NMOS devices and preferably comprising As or P, implanted with an energy of between about 2 to 60 KeV and a dose of between about 1E13 to 2E15 atoms/cm^2.

33. The method of claim 29, the LDD impurity implant being for PMOS devices and preferably comprising BF_2 or B, implanted with an

energy of between about 1 to 60 KeV and a dose of between about 1E13 to 2E15 atoms/cm^2.

34. The method of claim 29, the S/D implant being a N-type S/D region comprising As or P, implanted with an energy between about 10 and 100 KeV and a dose between about 1E14 to 5E16 atoms/cm^2.

35. The method of claim 29, the S/D implant being a P-type S/D region comprising boron or BF2, implanted with an energy between about 5 and 200 KeV and a dose between about 1E14 to 5E16 atoms/cm^2.

36. The method of claim 29, the etch blocking mask comprising photoresist.

37. The method of claim 29, the etch blocking mask comprising a pattern enlargement of a butt contact opening.

38. The method of claim 37, the enlargement comprising increasing a sizing rule for a butt contact opening by between about 0.005 and 0.2 μm.

39. The method of claim 37, the enlargement comprising photoresist overetch.